

# DATA SHEET

**74ALVT16646**

**2.5V/3.3V 16-bus transceiver (3-State)**

Product specification  
Supersedes data of 1996 Aug 13  
IC23 Data Handbook

1998 Feb 13

## 2.5V/3.3V 16-bit bus transceiver (3-State)

## 74ALVT16646

## FEATURES

- 16-bit universal bus interface
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74ALVT16646 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ( $\overline{OE}$ ) input for easy cascading and a Direction (DIR) input for direction control.

Data on the A or B bus is clocked into the registers on the Low to High transition of the appropriate clock (CPAB or CPBA). The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL		UNIT
			2.5V	3.3V	
$t_{PLH}$ $t_{PHL}$	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50\text{pF}$	2.2 2.3	1.7 1.8	ns
$C_{IN}$	Input capacitance DIR, $\overline{OE}$	$V_I = 0\text{V}$ or $V_{CC}$	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O} = 0\text{V}$ or $V_{CC}$	9	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled	40	70	$\mu\text{A}$

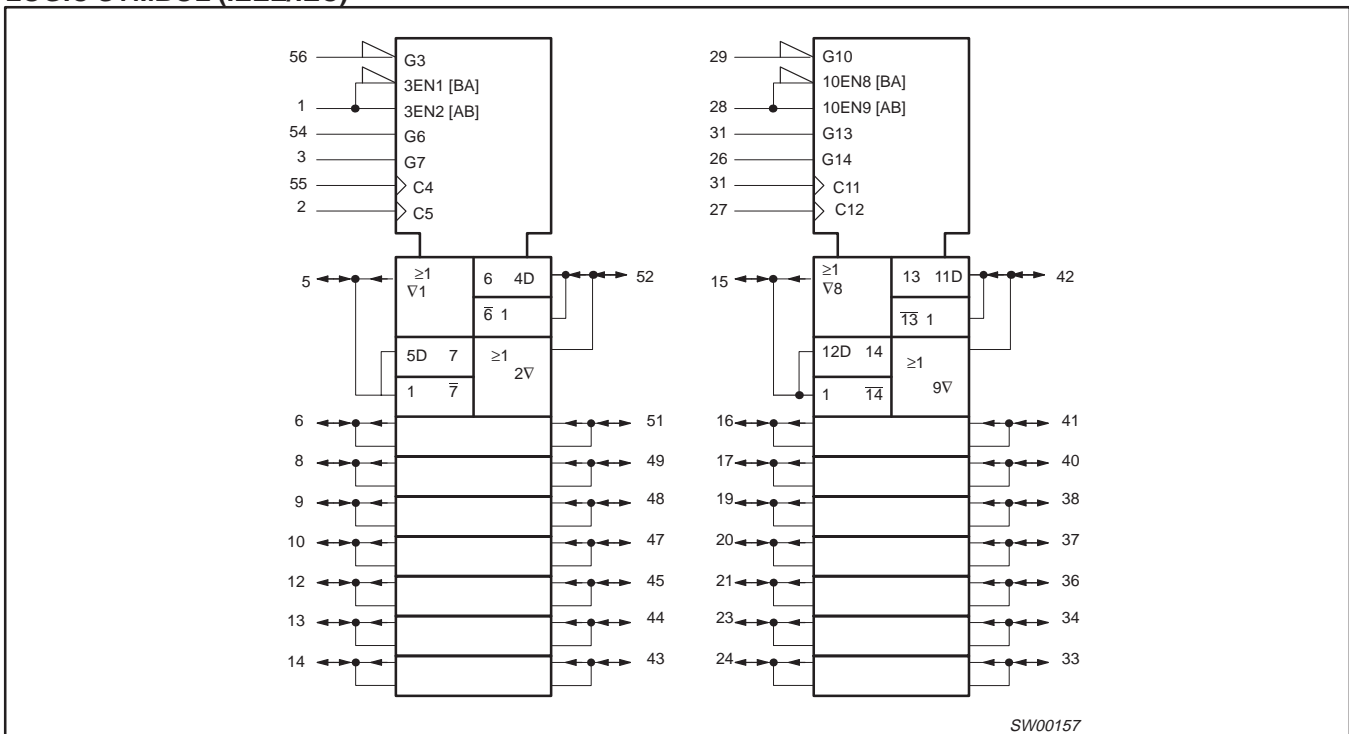
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ALVT16646 DL	AV16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVT16646 DGG	AV16646 DGG	SOT364-1

# 2.5V/3.3V 16-bit bus transceiver (3-State)

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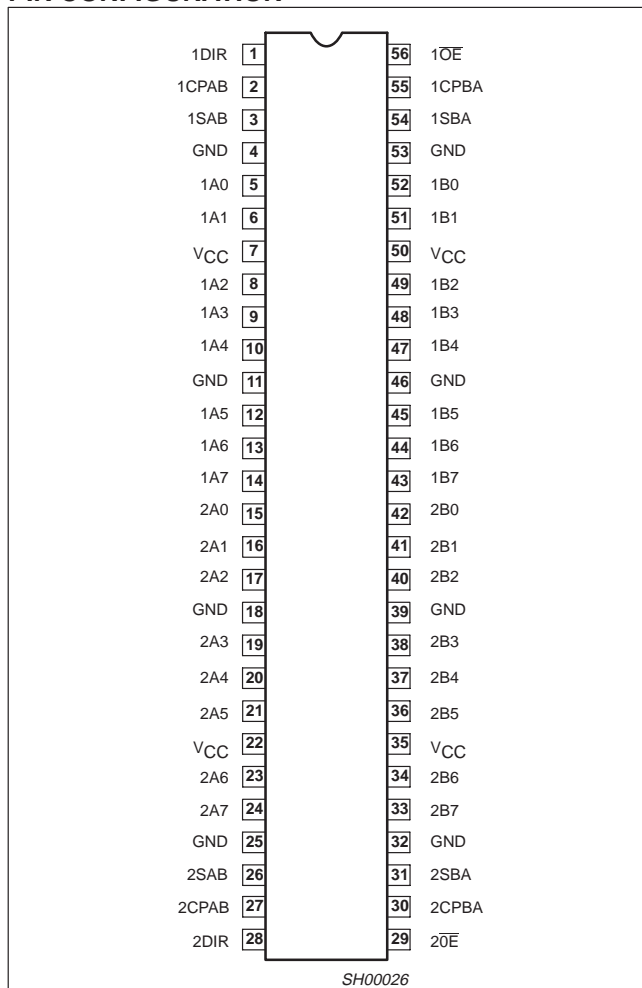
## LOGIC SYMBOL (IEEE/IEC)



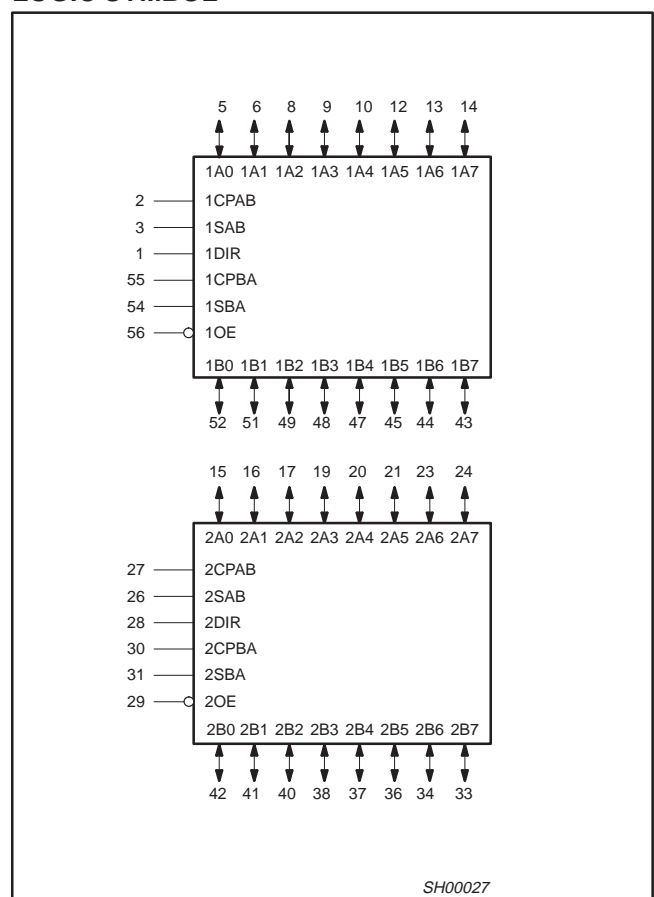
# 2.5V/3.3V 16-bit bus transceiver (3-State)

# 74ALVT16646

## PIN CONFIGURATION



## LOGIC SYMBOL



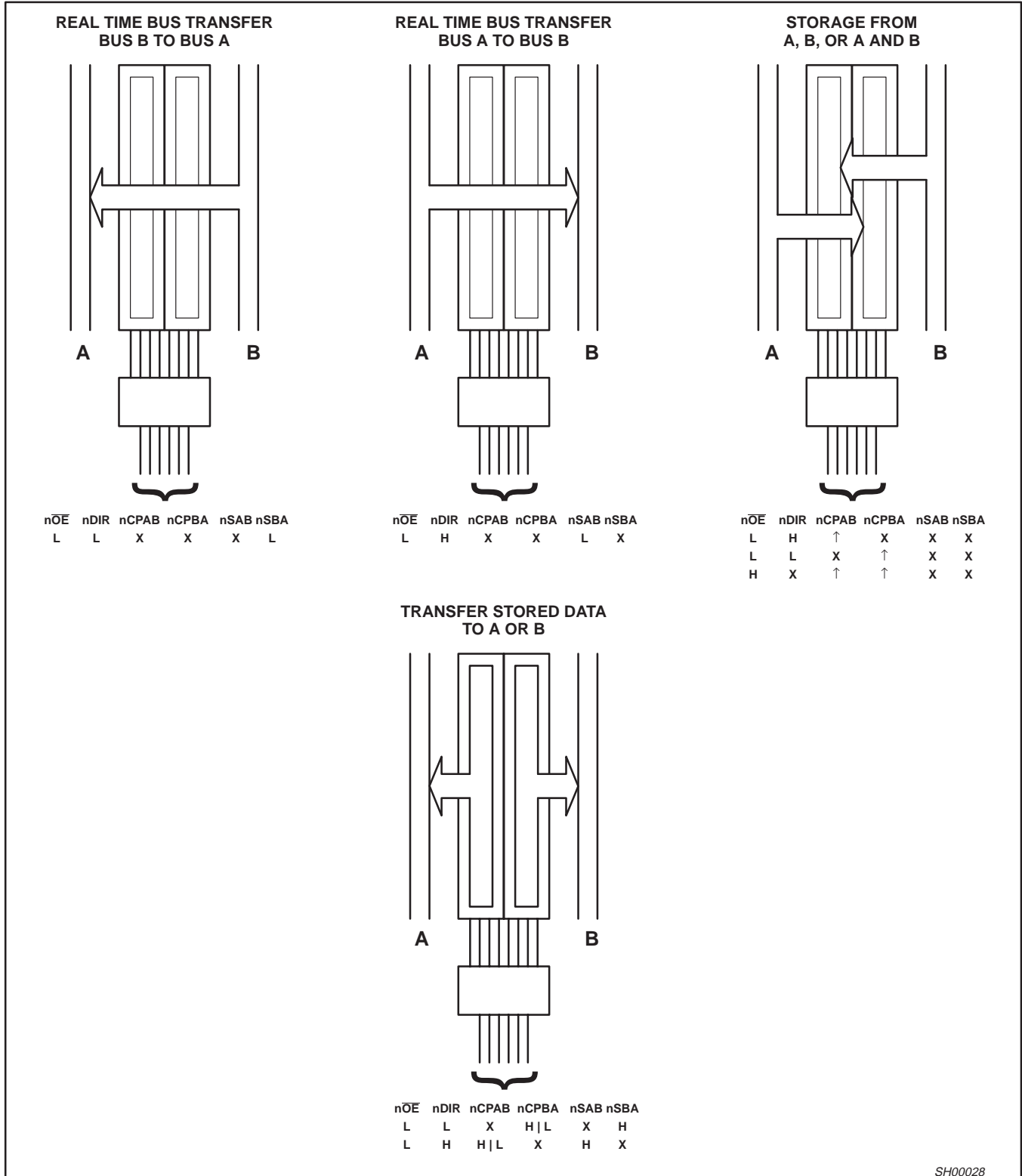
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 - 1A7, 2A0 - 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 - 1B7, 2B0 - 2B7	Data inputs/outputs (B side)
56, 29	1OE, 2OE	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	VCC	Positive supply voltage

# 2.5V/3.3V 16-bit bus transceiver (3-State)

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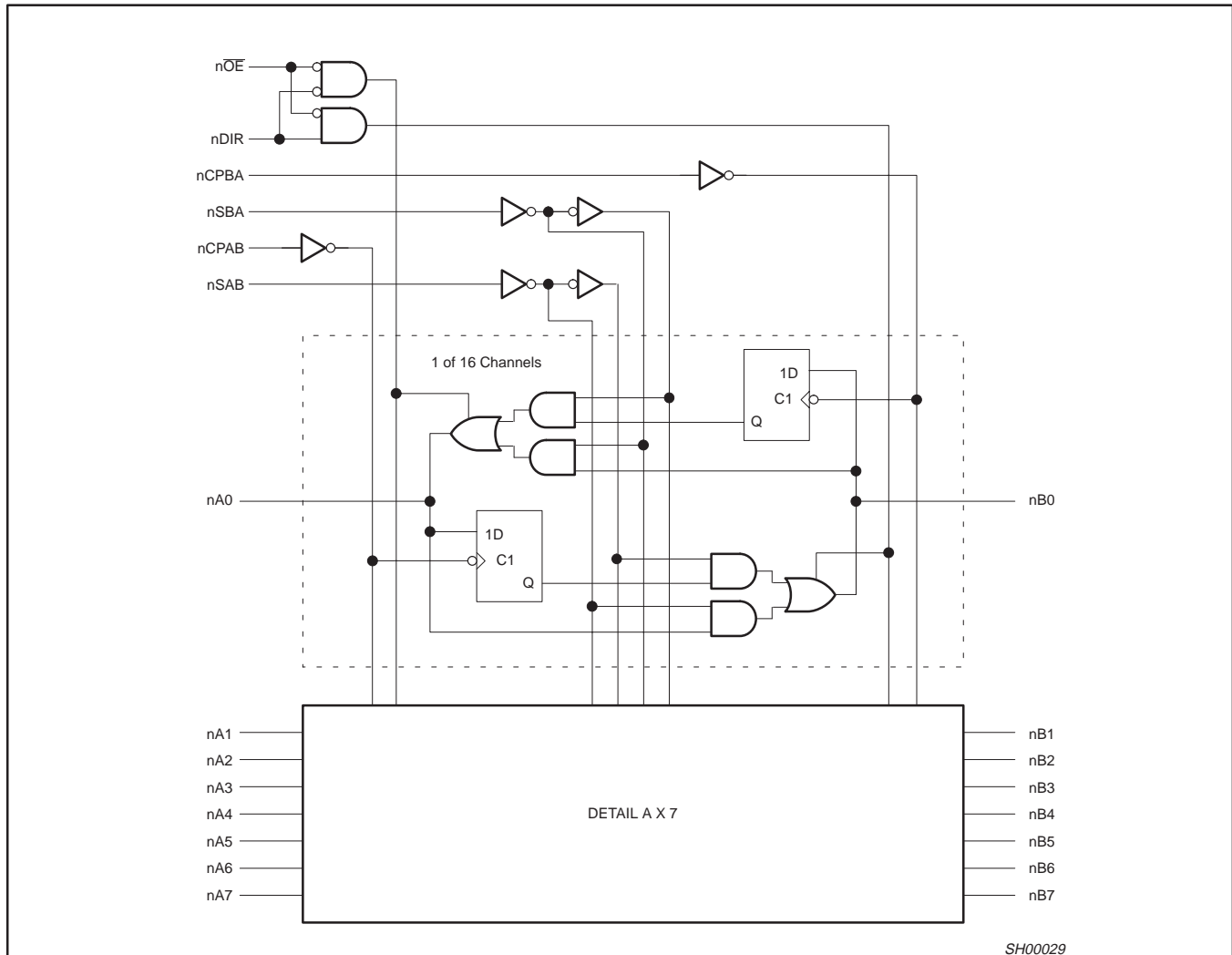
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALVT16646.



# 2.5V/3.3V 16-bit bus transceiver (3-State)

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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↑ = Low-to-High clock transition

\* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

## 2.5V/3.3V 16-bit bus transceiver (3-State)

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**NOTES:**

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.3	2.7	3.0	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>IH</sub>	High-level input voltage	1.7		2.0		V
V <sub>IL</sub>	Input voltage		0.7		0.8	V
I <sub>OH</sub>	High-level output current		-8		-32	mA
I <sub>OL</sub>	Low-level output current		8		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		24		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	-40	+85	°C

## 2.5V/3.3V 16-bit bus transceiver (3-State)

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DC ELECTRICAL CHARACTERISTICS (3.3V  $\pm$  0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 3.0V; I <sub>IK</sub> = -18mA		-0.85	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 3.0 to 3.6V; I <sub>OH</sub> = -100 $\mu$ A	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA	2.0	2.3		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 100 $\mu$ A		0.07	0.2	V
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA		0.4	0.55	
V <sub>RST</sub>	Power-up output low voltage <sup>6</sup>	V <sub>CC</sub> = 3.6V; I <sub>O</sub> = 1mA; V <sub>I</sub> = V <sub>CC</sub> or GND			0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	0.1	$\pm$ 1	$\mu$ A
		V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		0.1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V	I/O Data pins <sup>4</sup>	0.1	20	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>		0.5	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		0.1	-5	
I <sub>OFF</sub>	Off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		0.1	$\pm$ 100	$\mu$ A
I <sub>HOLD</sub>	Bus Hold current Data inputs <sup>7</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	130		$\mu$ A
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-140		$\mu$ A
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0V to 3.6V	$\pm$ 500			$\mu$ A
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		50	125	$\mu$ A
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> $\leq$ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care		40	$\pm$ 100	$\mu$ A
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.07	0.14	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		3.2	7	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>5</sup>		0.07	0.14	
$\Delta$ I <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND		0.04	0.4	mA

## NOTES:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
- This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V  $\pm$  0.3V a transition time of 100 $\mu$ sec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
- Unused pins at V<sub>CC</sub> or GND.
- I<sub>CCZ</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.



## 2.5V/3.3V 16-bit bus transceiver (3-State)

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**AC CHARACTERISTICS (3.3V ± 0.3V RANGE)**GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$			
			MIN	TYP <sup>1</sup>	MAX	
$f_{\text{MAX}}$	Maximum clock frequency	1	150			MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	2.6 2.1	3.7 3.1	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nSAB to nBx or nSBA to nAx	2	1.0 1.0	2.4 2.1	4.0 3.8	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nAx to nBx or nBx to nAx	2 3	0.5 0.5	1.7 1.8	2.4 2.8	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	5 6	0.5 0.5	2.3 2.0	3.9 4.4	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low Level	5 6	1.5 1.5	3.4 2.8	5.0 4.2	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time nDIR to nAx or nBx	5 6	1.0 0.5	2.8 2.2	5.0 4.7	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time nDIR to nAx or nBx	5 6	1.5 1.0	3.5 3.1	5.4 4.7	ns

**NOTE:**1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .**AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)**GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 3.3V \pm 0.3V$		
			MIN	TYP <sup>1</sup>	
$t_S(\text{H})$ $t_S(\text{L})$	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.6 1.6	1.0 1.0	ns
$t_H(\text{H})$ $t_H(\text{L})$	Hold time, High or Low nAx to nCPAB or nBx or nCPBA	4	0.0 0.0	-0.5 -0.7	ns
$t_W(\text{H})$ $t_W(\text{L})$	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

**NOTE:**

1. This data sheet limit may vary among suppliers.

## 2.5V/3.3V 16-bit bus transceiver (3-State)

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## DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.3V; I <sub>IK</sub> = -18mA		-0.85	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -8mA	1.8	2.1		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 100μA		0.07	0.2	V
		V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 24mA		0.3	0.5	
		V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 8mA			0.4	
V <sub>RST</sub>	Power-up output low voltage <sup>7</sup>	V <sub>CC</sub> = 2.7V; I <sub>O</sub> = 1mA; V <sub>I</sub> = V <sub>CC</sub> or GND			0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	0.1	±1	μA
		V <sub>CC</sub> = 0 or 2.7V; V <sub>I</sub> = 5.5V		0.1	10	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = 5.5V	I/O Data pins <sup>4</sup>	0.1	20	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>CC</sub>		0.1	10	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = 0		0.1	-5	
I <sub>OFF</sub>	Off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		0.1	±100	μA
I <sub>HOLD</sub>	Bus Hold current A or B inputs <sup>6</sup>	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V		90		μA
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V		-10		μA
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 2.3V		50	125	μA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OĒ = Don't care		40	100	μA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 2.7V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.04	0.1	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 2.7V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		2.3	4.5	
I <sub>CCZ</sub>		V <sub>CC</sub> = 2.7V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>5</sup>		0.04	0.1	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 2.3V to 2.7V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND		0.01	0.4	mA

## NOTES:

- All typical values are at V<sub>CC</sub> = 2.5V and T<sub>amb</sub> = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.
- This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 2.5V ± 0.2V a transition time of 100μsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
- Unused pins at V<sub>CC</sub> or GND.
- I<sub>CCZ</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

# 2.5V/3.3V 16-bit bus transceiver (3-State)

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## AC CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP <sup>1</sup>	MAX	
$f_{\text{MAX}}$	Maximum clock frequency	1	150			MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.0 1.0	3.2 2.8	4.8 4.2	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nSAB to nBx or nSBA to nAx	2	1.5 1.5	3.4 3.4	5.8 6.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nAx to nBx or nBx to nAx	2 3	0.5 0.5	2.2 2.3	3.2 3.8	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	5 6	1.5 1.0	3.4 2.7	5.8 6.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low Level	5 6	1.5 1.0	3.2 2.5	5.2 3.7	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time nDIR to nAx or nBx	5 6	2.0 1.0	4.1 2.5	7.0 4.1	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time nDIR to nAx or nBx	5 6	1.5 1.0	3.9 3.1	6.1 4.9	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

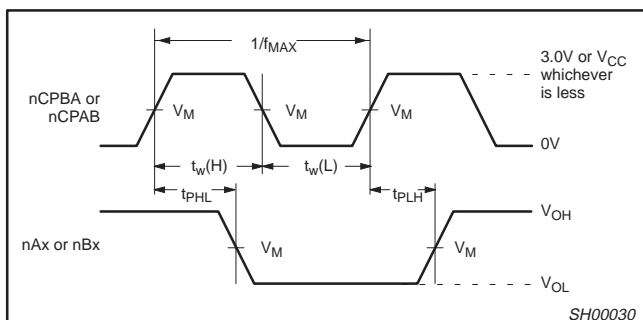
## AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

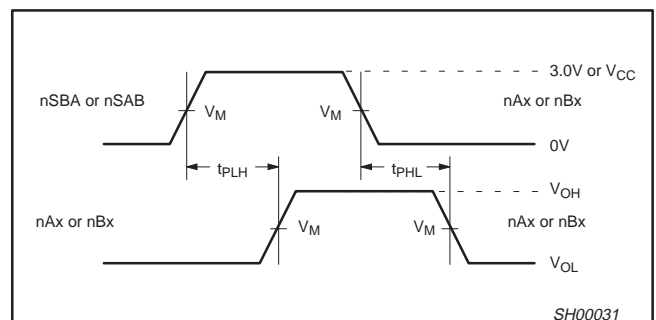
SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 2.5V \pm 0.2V$		
			MIN	TYP	
$t_S(\text{H})$ $t_S(\text{L})$	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	2.0 2.0	1.2 1.2	ns
$t_H(\text{H})$ $t_H(\text{L})$	Hold time, High or Low nAx to nCPAB or nBx or nCPBA	4	0.0 0.0	-1.0 -1.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	Pulse width, High or Low nCPAB or nCPBA	1	1.5 1.5		ns

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 3.0V$ ;  $V_M = V_{CC}/2$  at  $V_{CC} \leq 2.7V$   
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 3.0V$ ;  $V_X = V_{OL} + 0.15V$  at  $V_{CC} \leq 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 3.0V$ ;  $V_Y = V_{OH} - 0.15V$  at  $V_{CC} \leq 2.7V$



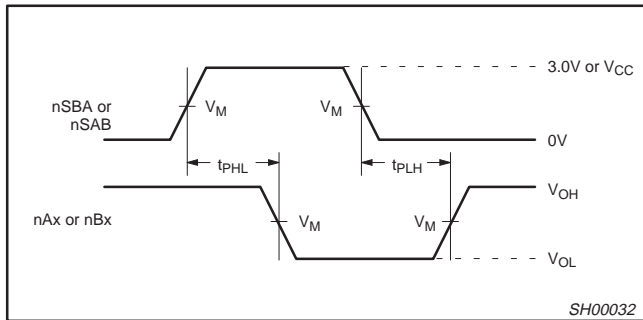
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



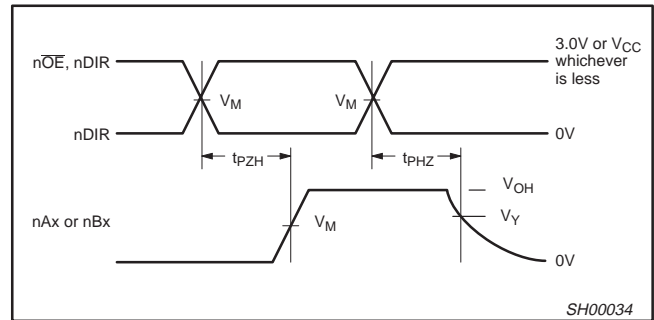
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx

# 2.5V/3.3V 16-bit bus transceiver (3-State)

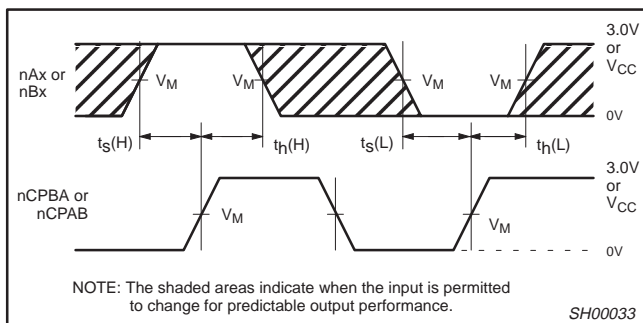
# 74ALVT16646



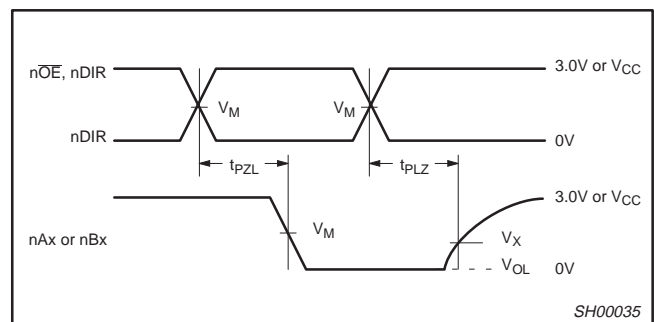
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}/t_{PZL}$	6V or $V_{CC} \times 2$
$t_{PLH}/t_{PHL}$	Open
$t_{PHZ}/t_{PZH}$	GND

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SW00025

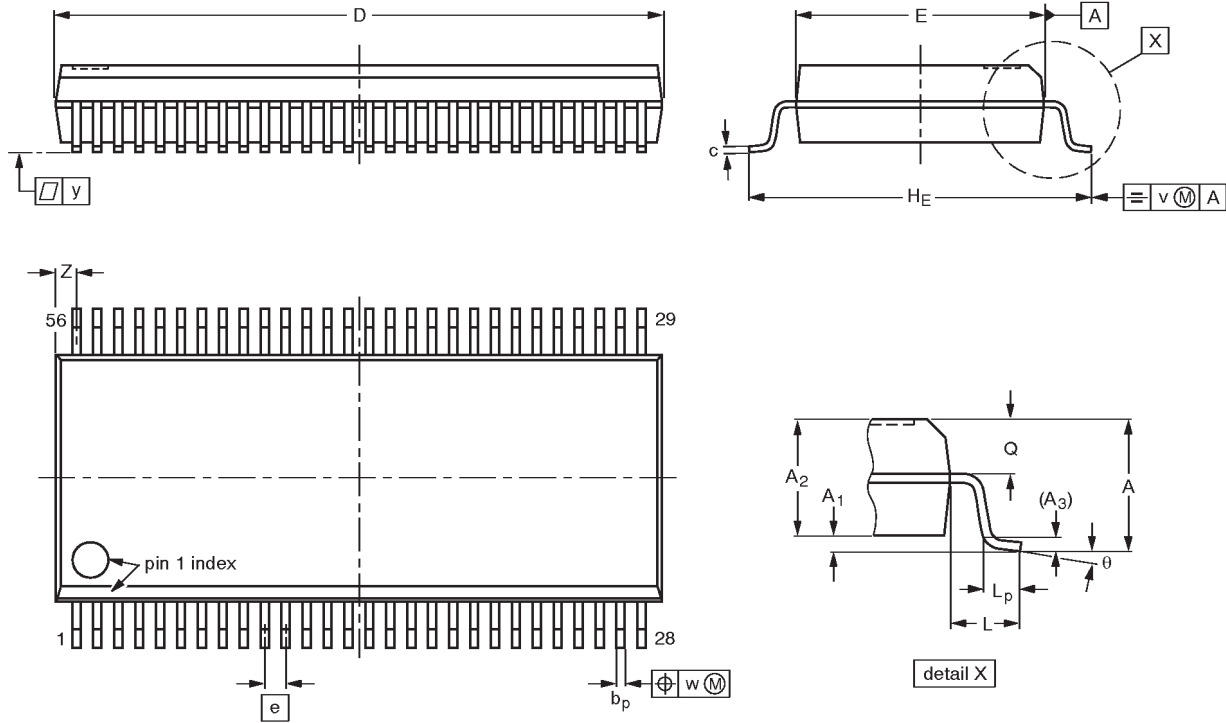
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ALVT16	3.0V or $V_{CC}$ whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

2.5V/3.3V 16-bit bus transceiver (3-State)

74ALVT16646

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

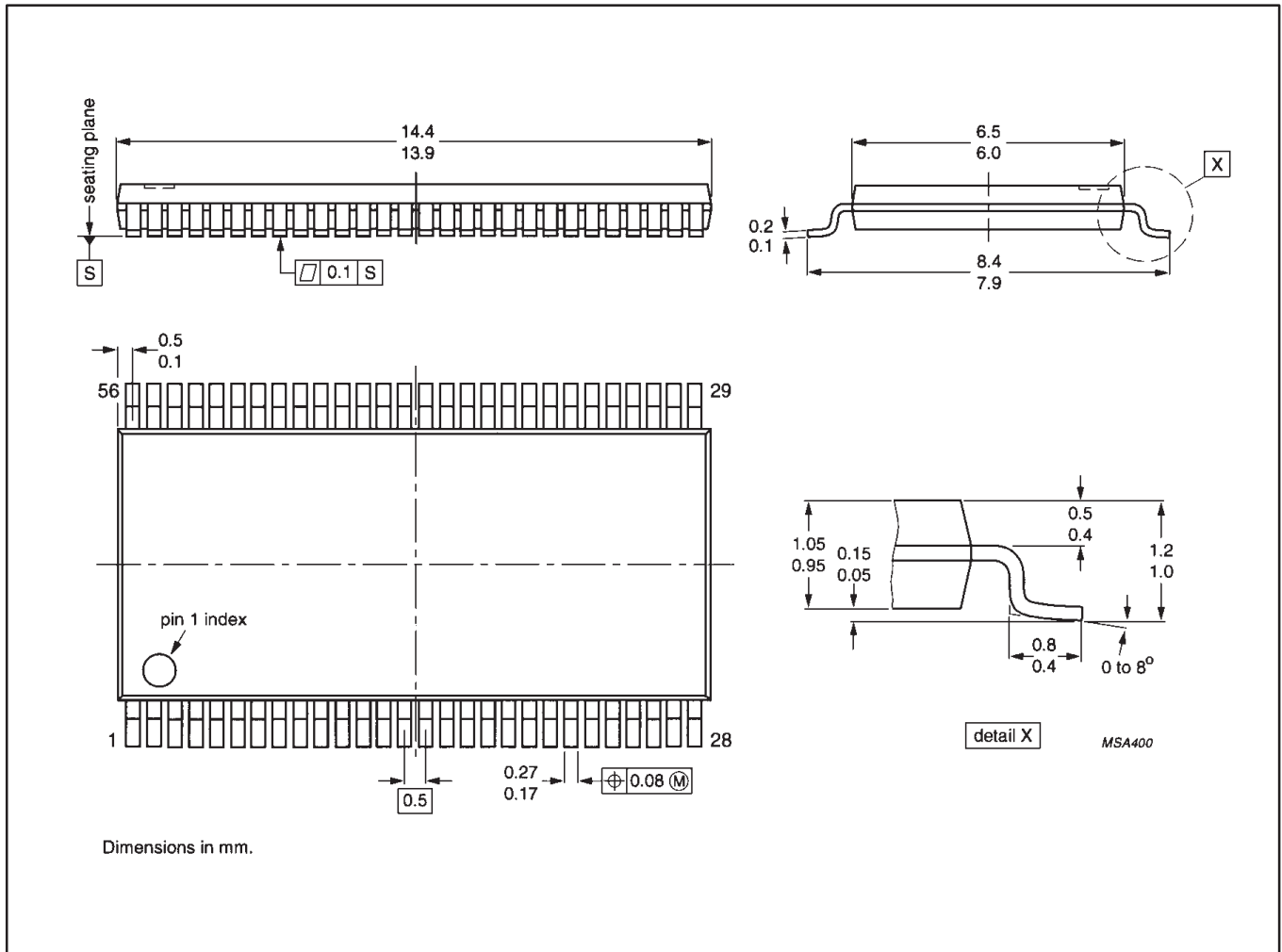
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

# 2.5V/3.3V 16-bit bus transceiver (3-State)

## 74ALVT16646

**TSSOP56:** plastic thin shrink small outline package; 56 leads; body width 6.1mm

**SOT364-1**



## 2.5V/3.3V 16-bit bus transceiver (3-State)

74ALVT16646

**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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